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EXAMINER	
TIMORY, KABIR A	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,500	WANG, PING-YING	
	Examiner	Art Unit	
	Kabir A. Timory	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pitzer et al. (US Patent Number 6,876,710) in view of Kim et al. (US Pub. Number 2004/0001600).

Regarding claim 1:

As shown in figure 1A, Pitzer et al. discloses a clock generator circuit, comprising:

- a multi-phase clock signal generator (figure 1A, 12) for generating a plurality of clock signals having a same frequency but difference phases according to a reference clock signal (figure 1A, REF-CLK);
- a modulation device for generating a phase modulation signal through Delta-Sigma modulation (figure 1A, 26); and
- a phase modulator, which is electrically coupled to the modulation device, for selecting (figure 1A, 14) (the multiplexer is interpreted to perform the selecting from plurality of multiphase clock signal and output one signal. Please see figure 1A for

more details) one of the clock signals to be a modulated clock signal according to the phase modulation signal (phase modulation is included in the Sigma-Delta Modulation) (figure 1A, 26, column 1, lines 19-22, column 5, lines 16-20).

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching signals having a same frequency but difference phases according to a reference clock signal.

However, Kim et al., in the same field of endeavor, teaches signals having a same frequency but difference phases according to a reference clock signal (clock signal having the same period is interpreted to be the signals having the same frequency) (paragraph 0025, lines 1-5).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system, in order to avoid signal overlapping, the generated clock signal which have the same period or frequency, should be different or shifted in phase. To overcome the overlapping, it would have been obvious to one ordinary skill in the art at the time the invention was made to shift the phase of signal as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. Multiple generated clock signal which have the same frequency but different phases in advantageous because by shifting the phase of generated clock signal we can avoid signal overlapping in the system.

Regarding claim 2:

Pitzer et al. further discloses, wherein the modulation device further comprises a modulation value generator for generating a modulation value and a Delta-Sigma

modulator for generating the phase modulation signal according to the modulation value (figure 3, 26, column 5, lines 16-22).

Regarding claim 3:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching wherein the modulation value is for controlling the average frequency of the modulated clock signal.

However, Kim et al., in the same field of endeavor, teaches wherein the modulation value is for controlling the average frequency of the modulated clock signal (figure 1, 16).

One of ordinary skill in the art would have clearly recognized that in order to control the amplitude of the signal or frequency VCO (voltage controlled oscillator) are used. A voltage controlled oscillator or VCO is an electronic oscillator specifically designed to be controlled in oscillation frequency by a voltage input. To control frequency voltage oscillation, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a VCO in the system as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. Advantageously, by using a VCO we can control the oscillation or rate of repetition of the modulated signal in the system.

Regarding claim 4:

Pitzer et al. further discloses, wherein the modulation value generator is for generating a modulation value according to the modulated clock signal (figure 1A, 26).

Regarding claim 5:

Pitzer et al. further discloses, further comprising a divider for dividing the modulated clock signal and outputting to the modulation value generator (figure 1A, 30).

Regarding claim 6:

Pitzer et al. further discloses, wherein the multi-phase clock signal generator is a first phase-locked loop (figure 1A, 12).

Regarding claim 7:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching wherein the first phase-locked loop comprises a phase frequency detector, a charge pump, a loop filter, and a voltage controlled oscillator.

However, Kim et al., in the same field of endeavor, teaches wherein the first phase-locked loop comprises a phase frequency detector, a charge pump, a loop filter, and a voltage controlled oscillator (figure 1, 10, 12, 14, 16).

One of ordinary skill in the art would have clearly recognized that a phase-locked loop (PLL) is a closed-loop feedback control system that generates and outputs a signal in relation to the frequency and phase of an input "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. Usually, a PLL is consists of phase frequency detector, a charge pump, a loop filter, and a voltage controlled oscillator. In order to generates and outputs a signal in relation to the frequency and phase of a reference signal, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a PLL circuit as taught by Kim et al. in phase

locked loop for reducing electromagnetic interference and control method. Including the PLL circuitry in the system id advantageous because we can stabilize a generated signal or to detect signals in the presence of noise.

Regarding claim 8:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching wherein the phase modulator comprises: a phase selector for selecting two clock signals out of the clock signals; and
a phase interpolator for outputting the modulated clock signal according to the two clock signals through phase interpolation.

However, Kim et al., in the same field of endeavor, teaches wherein the phase modulator comprises: a phase selector (clock selecting portion is interpreted to be the phase selector) (figure 1, 20) for selecting two clock signals out of the clock signals (paragraph 0029, lines 1-6); and a phase interpolator (figure 1, 18) for outputting the modulated clock signal according to the two clock signals through phase interpolation (paragraph 0031, lines 6-7).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system in order to select clock signals among plurality of clock signals, a clock or phase selector is required. Also to generate phase-shifted signals, an interpolator is used in the system. Interpolator receives the clock signal and generates first through n-th discrete clock signals having the same period but shifted in phase by predetermined offsets so as to not to overlap one another. In order to select and generate phase-shifted signals, it would have been obvious to one ordinary skill in the

art at the time the invention was made to include a phase selector and an interpolator as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including phase selector and interpolator, we can generate phase-shifted signals and select the desired clock signals in the system.

Regarding claim 9:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching, wherein the phase of the two clock signals is adjacent.

However, Kim et al., in the same field of endeavor, teaches wherein the phase of the two clock signals is adjacent (figure 3).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system in order to aviod signal overlaping the clock signals need to be adjacent to one another. These clock signals may have the same period or frequency but are shifted in phase. To avoid signal overlapping, it would have been obvious to one ordinary skill in the art at the time the invention was made to include an offset between any two adjacent ones of the shifted clock signals as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including an offset we can assure the adjacency between two or more clock signals and generating non-overlapping signal.

Regarding claim 10:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching wherein the phase modulator comprises: a phase interpolator for generating a plurality of phase-interpolated clock signal according to the clock signals

through phase interpolation; and a phase selector for selecting one of the phase-interpolated clock signal to be the modulated clock signal.

However, Kim et al., in the same field of endeavor, teaches wherein the phase modulator comprises: a phase interpolator (figure 1, 18) for generating a plurality of phase-interpolated clock signal according to the clock signals through phase interpolation (paragraph 0031, lines 6-7); and a phase selector (clock selecting portion is interpreted to be the phase selector) (figure 1, 20) for selecting one of the phase-interpolated clock signal to be the modulated clock signal paragraph 0029, lines 1-6).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system in order to select clock signals among plurality of clock signals, a clock or phase selector is required. Also to generate phase-shifted signals, an interpolator is used in the system. Interpolator receives the clock signal and generates first through n-th discrete clock signals having the same period but shifted in phase by predetermined offsets so as to not to overlap one another. In order to select and generate phase-shifted signals, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a phase selector and an interpolator as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including phase selector and interpolator, we can generate phase-shifted signals and select the desired clock signals in the system.

Regarding claim 11:

As shown in figure 1A, Pitzer et al. discloses A method for generating a modulated clock signal, comprising the steps of:

- generating a plurality of clock signals having a same frequency but difference phases according to a reference clock signal (figure 1A, 12, REF-CLK);
- generating a phase modulation signal through Delta-Sigma modulation (figure 1A, 26);
- outputting a modulated clock signal through selecting one of the clock signals according to the phase modulation signal (figure 1A, 26, column 5, lines 16-20).

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching signals having a same frequency but difference phases according to a reference clock signal.

However, Kim et al., in the same field of endeavor, teaches signals having a same frequency but difference phases according to a reference clock signal (clock signal having the same period is interpreted to be the signals having the same frequency) (paragraph 0025, lines 1-5).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system, in order to avoid signal overlapping, the generated clock signal which have the same period or frequency, should be different or shifted in phase. To overcome the overlapping, it would have been obvious to one ordinary skill in the art at the time the invention was made to shift the phase of signal as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. Multiple generated clock signal which have the same frequency but different phases in advantageous because by shifting the phase of generated clock signal we can avoid signal overlapping in the system.

Regarding claim 12:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching, wherein an average frequency of the modulated clock signal is controlled by adjusting the modulation signal.

However, Kim et al., in the same field of endeavor, teaches wherein an average frequency of the modulated clock signal is controlled by adjusting the modulation signal (figure 1, 16).

One of ordinary skill in the art would have clearly recognized that in order to control the amplitude of the signal or frequency VCO (voltage controlled oscillator) are used. A voltage controlled oscillator or VCO is an electronic oscillator specifically designed to be controlled in oscillation frequency by a voltage input. To control frequency voltage oscillation, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a VCO in the system as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. Advantageously, by using a VCO we can control the oscillation or rate of repetition of the modulated signal in the system.

Regarding claim 13:

Pitzer et al. further discloses, a detection step of determining a value of the modulation signal by detecting the modulated clock signal (edge detector is interpreted to detection step) (figure 1A, 32).

Regarding claim 14:

Pitzer et al. further discloses, wherein the step of outputting the modulated clock signal comprises: selecting (multiplexer in interpreted to do the signal selecting) (figure 1A, 14) two clock signals out of the clock signals; and outputting the modulated clock signal according to the two clock signals through phase interpolation (the modulator 26 is outputting 2 signals) (figure 1A, 26).

Regarding claim 15:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching, wherein the phase of the two clock signals is adjacent.

However, Kim et al., in the same field of endeavor, teaches wherein the phase of the two clock signals is adjacent (figure 3).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system in order to aviod signal overlaping the clock signals need to be adjacent to one another. These clock signals may have the same period or frequency but are shifted in phase. To avoid signal overlapping, it would have been obvious to one ordinary skill in the art at the time the invention was made to include an offset between any two adjacent ones of the shifted clock signals as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including an offset we can assure the adjacency between two or more clock signals and generating non-overlapping signal.

Regarding claim 16:

Pitzer et al. discloses all of the subject matter as described above except for specifically teaching, wherein the step of outputting the modulated clock signal

comprises: generating a plurality of phase-interpolated clock signal according to the clock signals through phase interpolation; and selecting one of the phase-interpolated clock signal to be the modulated clock signal.

However, Kim et al., in the same field of endeavor, teaches wherein the step of outputting the modulated clock signal comprises: generating a plurality of phase-interpolated clock signal according to the clock signals through phase interpolation (figure 1, 18); and selecting one of the phase-interpolated clock signal to be the modulated clock signal (figure 1, 20).

One of ordinary skill in the art would have clearly recognized that in a multiphase clock generating system in order to select clock signals among plurality of clock signals, a clock or phase selector is required. Also to generate phase-shifted signals, an interpolator is used in the system. Interpolator receives the clock signal and generates first through n-th discrete clock signals having the same period but shifted in phase by predetermined offsets so as to not to overlap one another. In order to select and generate phase-shifted signals, it would have been obvious to one ordinary skill in the art at the time the invention was made to include a phase selector and an interpolator as taught by Kim et al. in phase locked loop for reducing electromagnetic interference and control method. By including phase selector and interpolator, we can generate phase-shifted signals and select the desired clock signals in the system.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Castiglione et al. (US Patent Number 7,079,616) discloses Process for generating a variable frequency signal, for instance for spreading the spectrum of a clock signal, and device therefor, Opsahl et al. (US Patent Number 5,903,194) discloses Digital phase modulation of frequency synthesizer using modulated fractional division, Fujiwara et al. (US Pub. Number 2002/0171457) discloses Method of generating a clock, a clock generation device, and electronic apparatuses having a clock generation device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kabir A. Timory whose telephone number is (571) 270-1674. The examiner can normally be reached on Mon - Thu 6:30AM - 4:00PM & Fri 6:30AM - 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kabir A. Timory
May 11, 2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER